FM/SW/MW/LW 33-BAND RADIO RECEIVER

CRF-330K

US Model
Canadian Model
E Model
AEP Model
UK Model

SUPPLEMENT

No. 2
February, 1978

File this supplement with the service manual.

CIRCUIT AND MECHANISM OPERATION

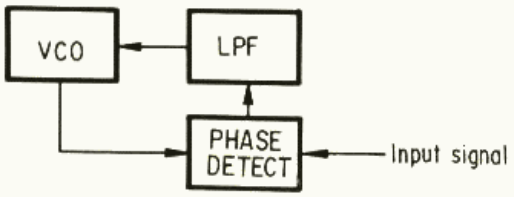
TABLE OF CONTENTS

SONY
SERVICE MANUAL

RADIO SECTION

1. PHASE–LOCKED LOOP

The phase-locked loop (PLL) is a type of frequency feedback circuit made up of a phase detector (PD), low-pass filter (LPF), and a voltage-controlled oscillator (VCO). The frequency of the VCO is synchrounized to the frequency of the input signal.

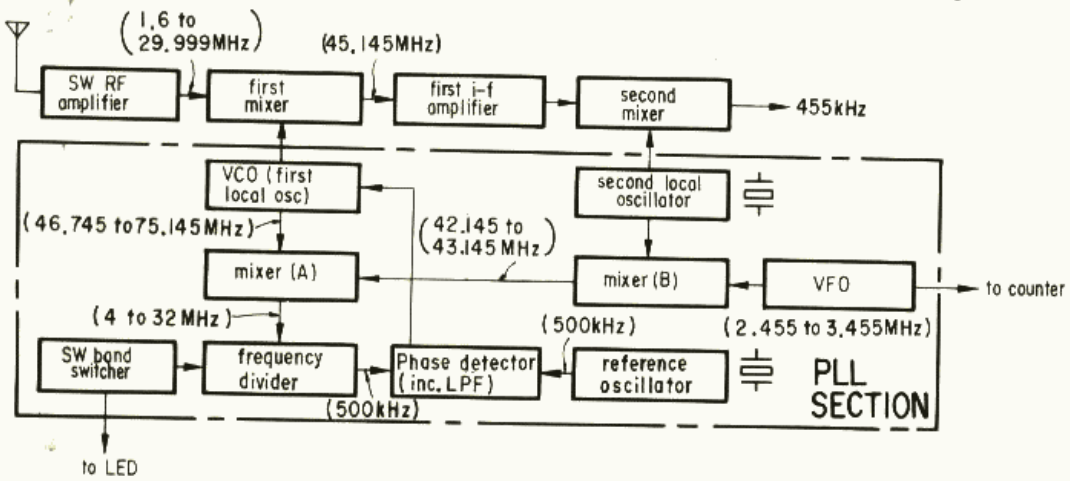


When there is no input signal, the VOC oscillates at its free-running frequency. When the input signal is received, the phase-detector compares the VCO oscillation frequency with the frequency of phase of the input signal. If they do not match, the phase detector detects the difference as a voltage signal. This voltage is changed into direct current by the LPF, and shifts the VCO frequency towards that of the input signal. When both frequencies are the same, the phase detector voltage becomes constant, thus synchronizing or locking the PLL. Under these conditions, the VCO oscillation output and the input signal will be of the same frequency with a constant phase difference.

2. THE PLL USED IN THIS RECEIVER

The PLL has been inserted in the short-wave local oscillator circuit to stabilize the oscillation frequency. As a result, the receiver is very stable.

If the output of the frequency divider is not at 500 kHz, the phase-detector generates and sends a voltage to the VCO, and controls the VCO frequency so that the frequency divider output will ultimately



In the above short-wave front-end block diagram, the signal received via the antenna is changed to a 45.145 MHz first i-f signal by the first mixer. After going through the i-f amplifier stage, it is converted to a 455 kHz second i-f signal at the second mixer.

In the PLL section, the output of the second local oscillator is mixed with the VFO output in the mixer (B). The mixer (B) output is equivalent to the input signal shown in the PLL diagram of section 1. It is mixed with the VCO output in the mixer (A). The mixer (A) output can be any frequency between 4 and 32 MHz, depending upon the frequency of the signal received. The output is then divided by the frequency divider, and compared with the 500 kHz signal of the reference oscillator at phase-detector.

be at 500 kHz. Thus, the VCO frequency is controlled by three oscillators (second local oscillator, VFO, and reference oscillator). The second local oscillator and the reference oscillator are both extremely stable crystal oscillators. The VFO is a stable lower frequency oscillator.

The amount of frequency division is selected by the band selector switch. The initial division is by 2, and then by from 4 to 32. Therefore, the VCO frequencies can be changed in 1 MHz steps by changing the ratio of the frequency divider, and in smaller steps by changing the VFO frequency. The VFO frequency is changed by turning the SW tuning knob.

1) Changing of the VCO Coils

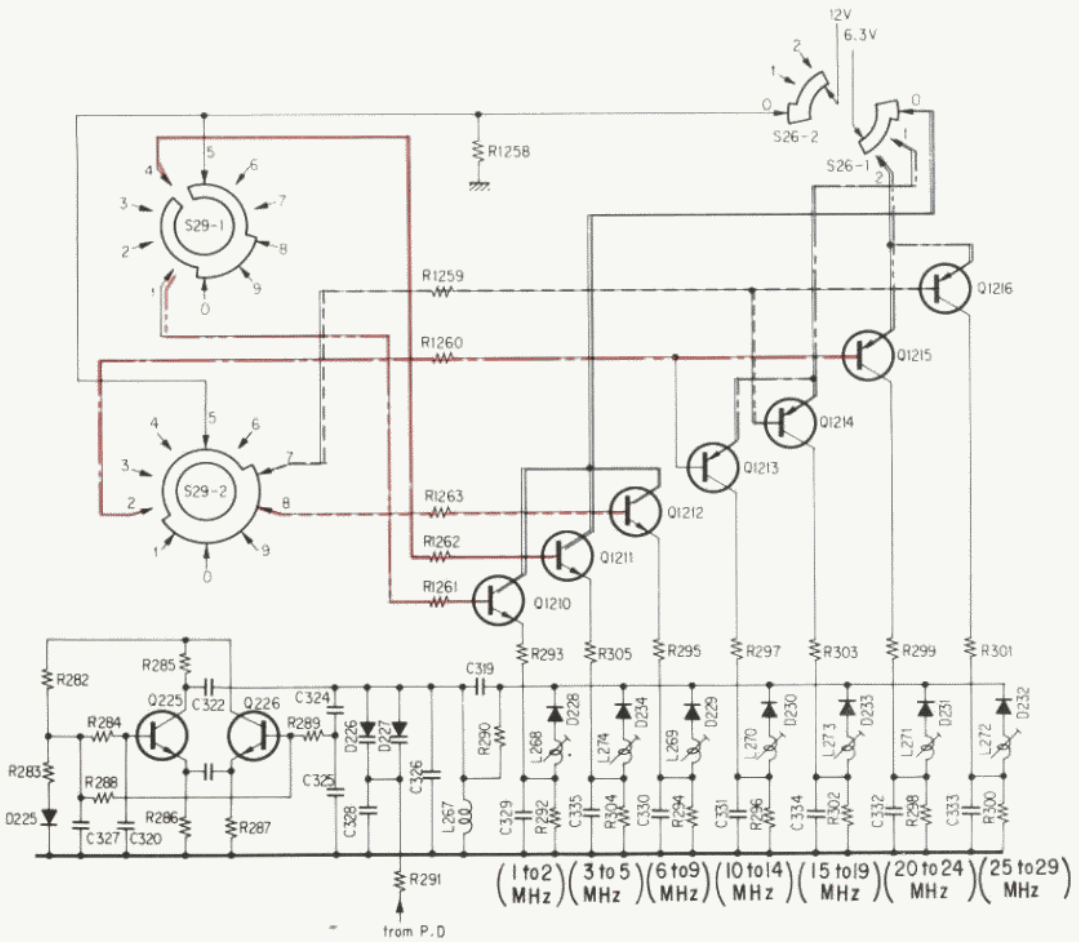
The VCO (voltage controlled oscillator) is equivalent to the local oscillator in the usual superheterodyne receiver. The difference between the VCO and the usual local oscillator lies in the tracking of the VCO, or more precisely, in the fact that the VCO frequency changes accurately according to the VFO frequency variations, and the divided VCO frequency is continually compared with the reference oscillator frequency so that the VCO is locked at a stable frequency. The VCO frequency is controlled via the variable capacitor diodes D226 and D227 in the diagram by the DC output from the phase detector (PD).

However, it is difficult to change the VCO frequency across the entire range by the variable capacitor diodes only. It is for this reason that, as shown in the diagram, a convenient division into 29 bands is made with switchable values of 'L' and the switching diodes D228 to D234. In the diagram, S26 is the switch for 10 MHz-interval band switching. It is turned progressively to the right (clockwise), in the order 0, 1, 2. S29 is the 1 MHz-interval switch, shown in position 9 in the diagram, from which it would be advanced successively to the right in the order 9, 0, 1 - - - - - - - - 8.

These two switches, S26 and S29, combine to give, for example, the 1 to 2 MHz band with Q1210 on. For the 1 to 2 MHz band, L268 enters the oscillator circuit as 'L'. In the same way, L274 gives the 3 to 5 MHz band, L269 gives the 6 to 9 MHz band, L270 the 10 to 14 MHz band, L273 the 15 to 19 MHz band, L271 the 20 to 24 MHz band, and L272 the 25 to 29 MHz band.

Note:

- B+ bus at 1 to 9 MHz band
- B+ bus at 10 to 19 MHz band
- B+ bus at 20 to 29 MHz band
- bias line path at 15 to 19 and 25 to 29 MHz bands
- bias line path at 10 to 14 and 20 to 24 MHz bands
- bias line path at 6 to 9 MHz band
- bias line path at 3 to 5 MHz band
- bias line path at 1 and 2 MHz bands

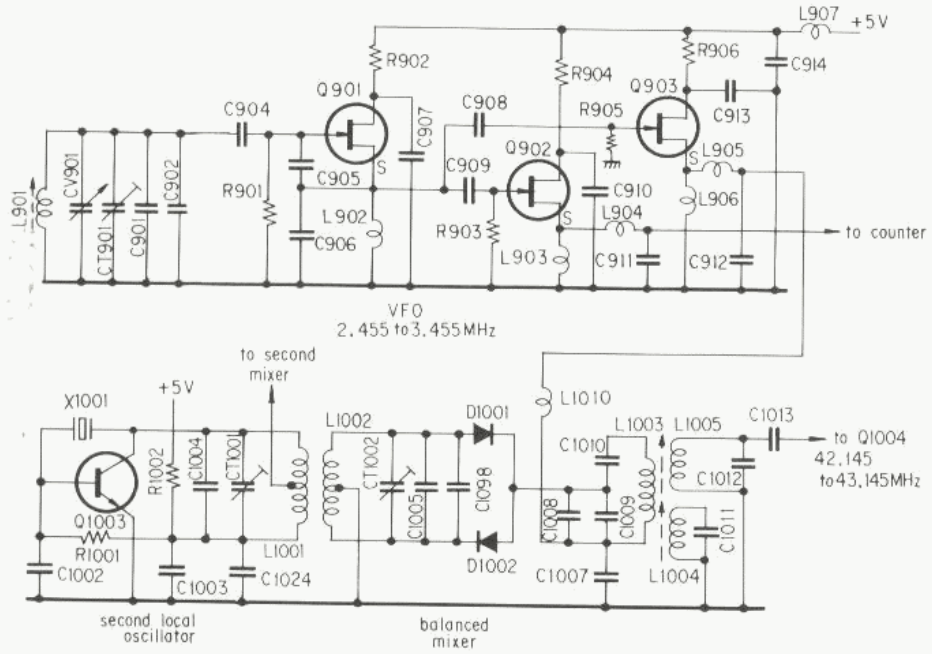


2) VFO

The stability of this set in short-wave reception is almost completely determined by the stability of the VFO. Of the three oscillators determining the stability of this set, the reference oscillator and the second local oscillator are fully stable crystal oscillators, and the VFO oscillator is at a low enough frequency (2.445 to 3.445 MHz) to permit highly stable circuit design. This is an advantageous characteristic feature of synthesizer receivers. The mixing of the VFO output and the output of the second local oscillator gives variable frequencies which are both high enough and stable enough for the purpose.

Again, by incorporating the output of the second local oscillator into the synthesizer loop, the instability in reception associated with second local oscillator drift is eliminated by the first and second mixers. Furthermore, the VFO frequency is measured by the counter, giving a display of all frequencies between the 1 MHz intervals.

As described above, the VFO block has been designed and selected with attention to detail for stability and precision. Repair and adjustment require special instrumentation and advanced techniques. Repairs should generally therefore be effected by block replacement.



3) Mixer (B) - - - - -D1001 and D1002

A part of the second local oscillator output (45.6 MHz) is mixed with the VFO output at D1001 and D1002 in order to boost the VFO frequency (2.455 to 3.455 MHz). The 2.455 to 3.455 MHz component of the mixer output is easily eliminated by the bandpass filter. Since 45.6 MHz is quite close to the frequency of the bandpass filter (42.145 to 43.145 MHz), the 45.6 MHz component leaks through the bandpass filter. In order to prevent the 45.6 MHz component from appearing at the output of the mixer, a balanced type mixer has been utilized. In a balanced type mixer, any frequency component of the signal inserted from the balanced side does not appear at the output side. Its operation can be thought of as a balanced type product detector.

4) Second Local Oscillator

The output of the second local oscillator is mixed with the first i-f signal at the second mixer and converted to the 455 kHz second i-f signal.

In this set, again, the output of the second local oscillator is incorporated into the synthesizer loop and applied to the first mixer. Therefore, the stability in reception associated with second local oscillator drift is cancelled by the first and second mixers.

5) Programmable Counter as Frequency Divider in PLL

A frequency divider can be composed of several counters. For example, in a decimal counter, then pulses input is converted to one pulse output. After all, the decimal counter operates as a 1/10 frequency divider. However, the division ratios required in this set are from 1/4 to 1/32. The two decimal counters including preset functions are installed for changing the division ratios, as shown in the diagram.

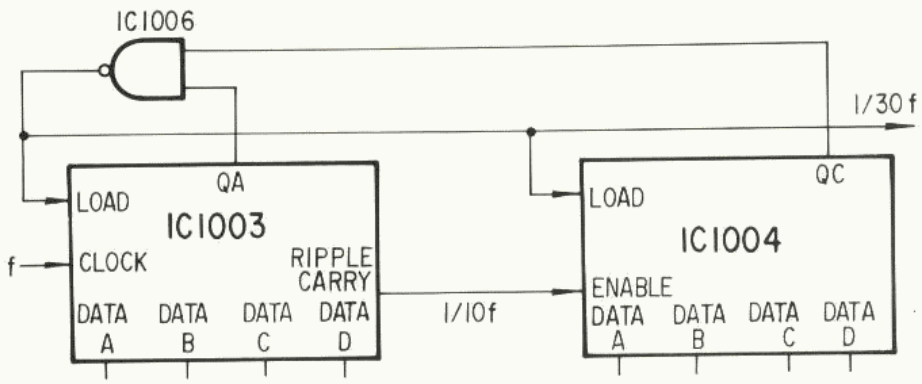
IC1003 and IC1004 are both programmable decimal counters and are capable of dividing up to 1/100. However, in this set, terminals C and D of IC1004 are grounded in order to obtain only a division of only 1/40. The output pulse of IC1006 is inputted at LOAD terminals of IC1003 and IC1004, and in so doing, the counters are reset. By this preset operation, the frequency divider circuit is actually capable of dividing up to 1/41.

The below table indicates the input and output combination of IC1003.

CLOCK input frequency	f	f	f	f	f
DATA A	0	1	0	0	0
DATA B	0	0	1	0	0
DATA C	0	0	0	1	0
DATA D	0	0	0	0	1
QA output frequency	0f (constantly LEVEL 1)	1/1 f	½ f	¼ f	1/8 f
RIPPLE CARRIER output frequency	1/10 f	1/10 f	1/10 f	1/10 f	1/10 f

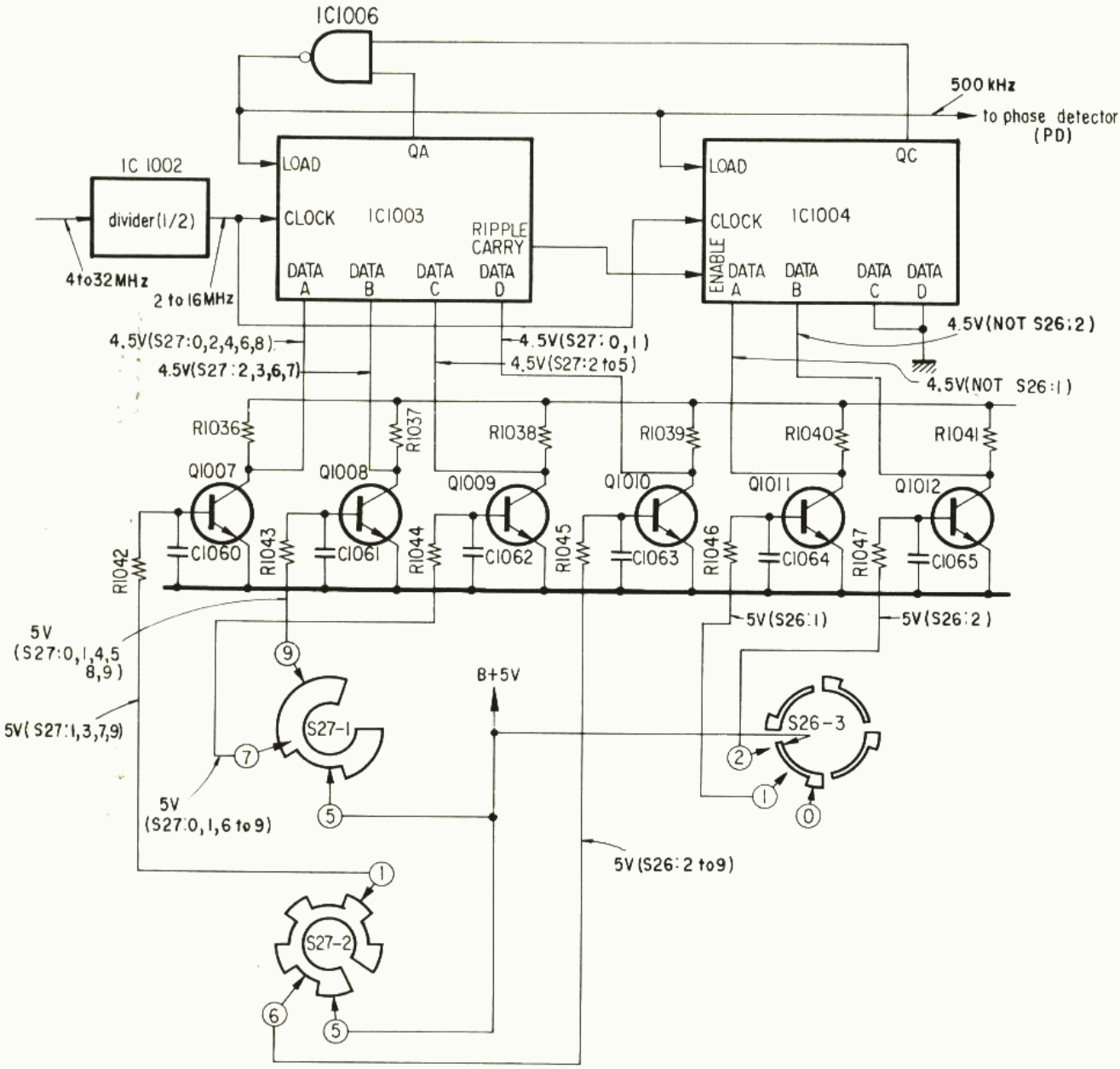
When the level of the DATA B is 1 and the levels of the DATA A, DATA C and DATA D are all 0, the CLOCK input frequency is divided by 2. The signal appears at the QA terminal. At this time, 8 has already been counted by IC1003 before the output signal from IC1002 enters the CLOCK terminal. In the same way, the division ratios change according to the levels of DATA terminals. Again, the RIPPLE CARRIER output frequency is always divided to 1/10 and inputted at the ENABLE terminal of IC1004. Thus, IC1004 counts 10, 20, 30 and 40.

The next diagram shows the frequency counter circuit, where 41 pulses are converted to one pulse. If division to 1/30 is required, preset the programmable counters to 11 by setting the DATA A levels of IC1003 and IC1004 to 1. This means that 11 has already been counted before inputting pulses at the CLOCK terminal of IC1003. Thus, when 30 pulses are inputted, this circuit counts 12 to 41 and one pulse appears as output. In other words, 30 pulses are converted to one pulse. Thus, the division to 1/30 is completed.



The below diagram shows the frequency divider circuit. The 4 to 32 MHz input is converted to a 2 to 16 MHz signal by IC1002. Again, the 2 to 16 MHz signal is converted to a 500 kHz signal, which is compared with the 500 kHz signal of the reference oscillator at PD, by IC1006, IC1003 and IC1004.

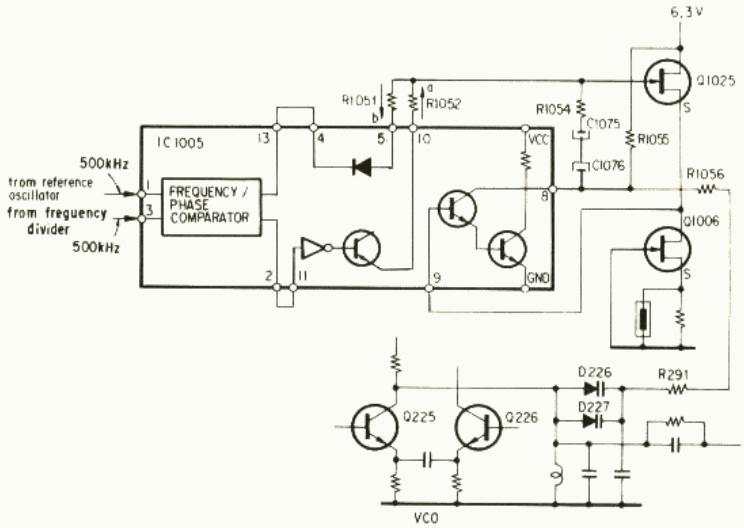
The output signal from IC1002 enters the CLOCK terminals of IC1003 and IC1004. The signal is not counted in IC1004, but synchronizes the counting in the two ICs. Q1007 to Q1012, S26-3, S27-1 and S27-2 constitute the control circuit for counter presetting.



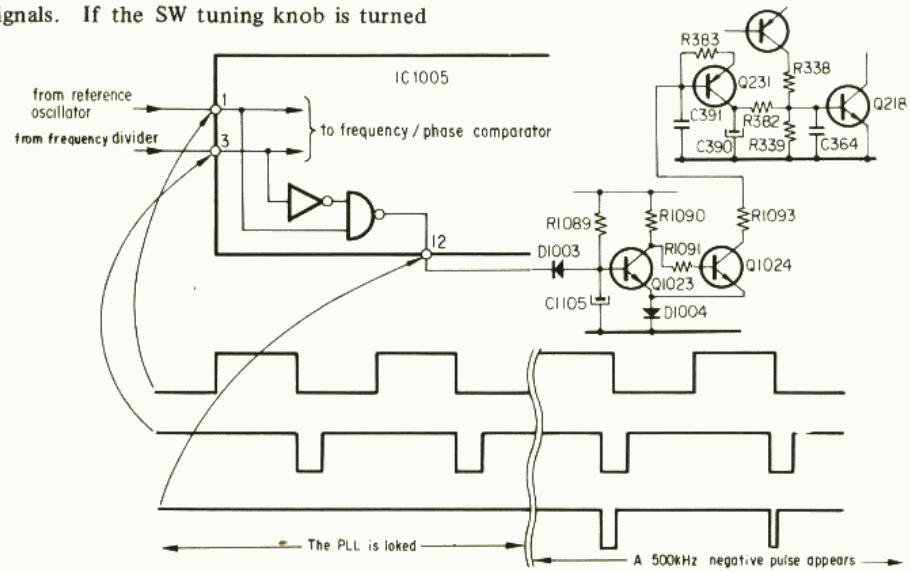
6) Phase Detector and Lowpass Filter

IC1005 is composed of a frequency/phase comparator and an integrator as shown below. When the output of the frequency divider is higher in frequency than the 500 kHz output of the reference oscillator, first the level at terminal 2 becomes 0 and then the level at terminal 10 becomes the high level. But, when it is lower, the level at terminal 13 becomes the low level and the level at terminal 8 becomes up to 6.3 V. Futhermore, the levels at both terminals 2 and 13 become the high levels, and the PLL is locked.

The signal from terminals 10 and 15 is integrated and amplified by the active lowpass filter. Next, this signal goes to the variable capacitance diodes D226 and D227, and controls the frequency of the VCO. When the PLL is locked, 1.75 V appears at terminal 8 in 1.6 MHz reception and 5 V appears in 29.999 MHz reception. Q1006 is a constant current load for Q1025.

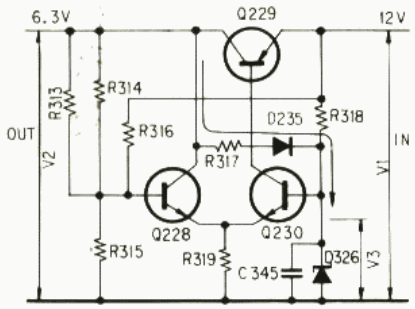


The next diagram shows that the duty factor of the signal from the reference oscillator is approx. 50%, and that of the divided to 1/4 signal from the frequency divider is 25%. When the PLL is locked, the level at terminal 12 is 1 as determined by the two input signals. If the SW tuning knob is turned during SW reception, the frequency of the signal from the frequency divider changes. Consequently, a 500 kHz negative pulse appears at terminal 12. This pulse is a trigger pulse for the muting operation of this set.



7) Regulator Circuit for VCO

If we assume that V2 has risen, the base voltage of Q228 will increase. This will increase the emitter current of Q228, and will raise the emitter voltage. At the same time, the emitter voltage of Q230 will increase and the emitter current will decrease, because the base voltage of Q230 is fixed by the zener diode D236. Therefore, the base current and collector current of Q229 will decrease, so that V2 will decrease a little and will be regulated. R316 is installed to prevent the influence of variation in V1 from affecting V2. Again, V3 is mainly applied via R317 and D235. However, with this alone, the regulator will not start to operate, and the start is effected by supplying an initial current to the base of Q230 via R318. D235 is inserted to prevent the initial current from flowing to the V2 side via R317.

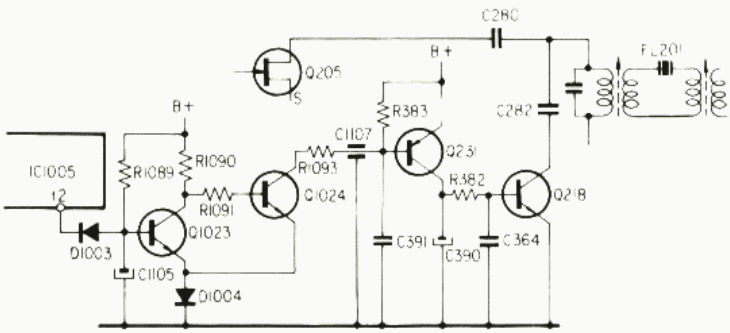


8) Muting Circuit Composed of Q1023, Q1024 and Q231.

When changing bands during SW reception, a small amount of time is required for the PLL to lock. Also, when the VCO frequency changes rapidly, noise will appear in the speaker. This muting circuit, composed of Q1023, Q1024 and Q231, is designed to mute the noise.

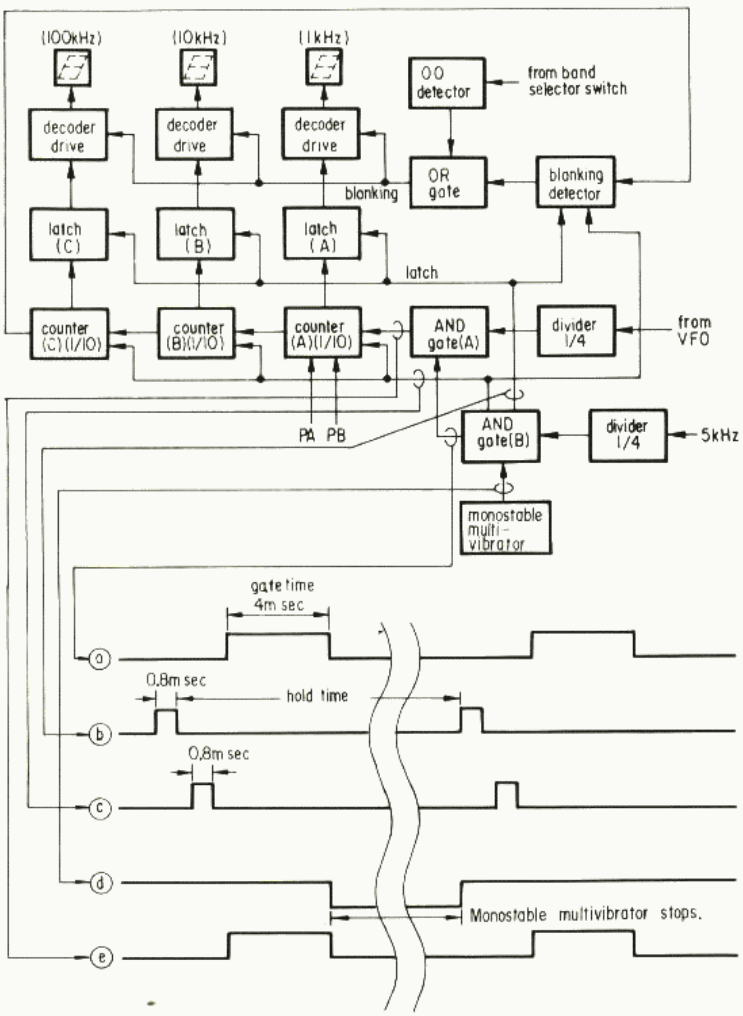
When the PLL is not locked, a 500 kHz negative pulse appears at terminal 12 of IC1005. This pulse is integrated at C1105, cutting off Q1023. Consequently, Q1024 comes on, and then Q231 comes on. Since the collector of Q231 is connected to the base of Q218 (noise blanker switch), Q218 comes on, and the i-f circuit is grounded. So long as it remains grounded, no sound will be heard from the speaker.

But once the PLL is locked, no further pulses will appear at terminal 12. Q1023 will then come on, and the muting operation will be terminated.



3. RECEIVED–SIGNAL FREQUENCY COUNTER

The display of frequencies between 1 MHz points is actually a display of counted VFO frequencies. The diagram shows a block diagram of the counter section. The input signals from the VFO are first divided to 1/4, and then passed onto the AND gate (A). The AND gate (A) is opened by the AND gate (B) for only 4 msec, since the VFO frequencies are divided by 4 and the displayed frequencies are in kHz, one cycle per msec. During this period, the VFO pulses which pass through the AND gate (A) are counted in the counters (A), (B) and (C). The AND gate (A) is closed after 4 msec, and the counters (A), (B) and (C) stop where they are. Pulse signals (b) from the AND gate (B) are then sent to the latches (A), (B) and (C), which in turn read off and memorize the values of the counters (A), (B) and (C). The counters are then restored to their original status by reset signals (c), ready to perform the next count. The decoders convert the binary numbers stored in the latches into decimal numbers for LED use, and then drive the LEDs via drive circuits. The latches maintain their status until the next latch pulse signals arrive. Consequently, the LED display is also maintained for the same length of time. As long as no signal from the monostable multivibrator is applied to the AND gate (B), the counters will again commence to count the next VFO signal after 4 msec. But since the pulses are counted once every 8 msec, even if the counter value varies a little, the LED display will change once every 8 msec, which is far too short to read frequencies. In order to prevent this, the AND gate (B) is switched off by the monostable multivibrator. The counters will then only count once every 100 msec.



Also incorporated in this set is a blanking circuit. Since reception is not possible when the SW BAND SELECTOR switch is at 00 with the VCO frequency outside the 3.455 to 2.455 MHz range, the frequency must not be displayed. Therefore, the 00 detector detects the 00 status of the SW BAND SELECTOR switch, and the blanking detector detects the counter status. These two outputs are passed through the OR gate, and extinguish the LEDs.

The below table shows the combination between the VFO frequencies and the received signal frequencies.

Received Signal	VFO Frequency	Low Three Figures of Received Signal Frequency (on SW Frequency Counter)
A3	3,455 kHz 3,454 kHz 2,456 kHz	000 kHz 001 kHz 999 kHz
USB	3,453.5 kHz 2,454.5 kHz	000 kHz 999 kHz
LSB, CW	3,456.5 kHz 2,457.6 kHz	000 kHz 999 kHz

When the VFO signal has a frequency down of 1 kHz, the received signal has a frequency up of 1 kHz. In A3 (AM mode) signal reception, when the low three figures of the VFO frequency are 455 kHz, that of the received signal frequency is 000 kHz. Therefore, at this time the counter is preset to 455 kHz. When the VFO frequency goes down, the received signal frequency goes up.

In the same way, the counter is preset to 454 kHz in USB signal reception and 456 kHz in LSB and CW signal reception. (0.5 of a kHz can not be counted.) In this set, then, the programmable down-counter is used to preset to 454, 455 and 456 kHz. The programmable down-counter is preset by the inputs via PA and PB as follows.

PA Level	PB Level	Presetting Frequency
low	low	454 kHz
high	low	455 kHz
low	high	456 kHz

1) IC1201

a) 1/2 IC1201

Gate of counter and ½ frequency divider. It has two operations as a T flip-flop.

If the input at terminal CD is used as a gate signal and keeps the terminal SD at 0 level, the level at the terminal CD becomes 0 and this circuit operates as a 1/2 frequency divider of a T flip-flop.

If the level at terminal CD becomes 1, the output at terminal Q becomes 0 and this operates as the counter gate of a RS flip-flop.

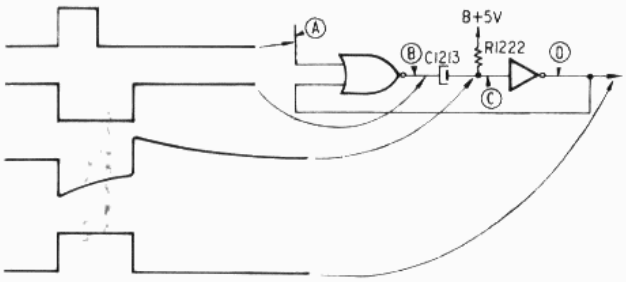
b) 2/2 IC1201

1/2 frequency divider of a T flip-flop with reset function.

2) IC1202

It consists of four NOR gates; two gates operate as an inverter. The other two gates operate as a monostable multivibrator as in the following figure.

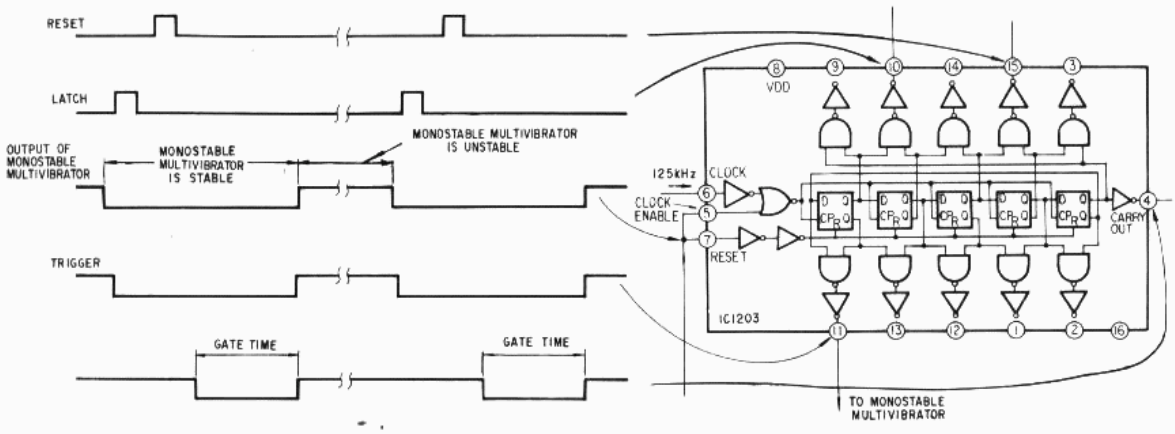
When a pulse is applied to Ⓐ, the voltage at Ⓑ and Ⓒ becomes low and the voltage at Ⓓ becomes high. But, the voltage at Ⓒ gradually increases to a high voltage according to the time constant determined by C1213 and R1222. Consequently the voltage at Ⓓ becomes low and the voltage at Ⓑ becomes high. At this time C1213 is discharged, so that the voltage at Ⓒ becomes too high and is gradually stabilized at 5V. This happens every time a pulse is applied to Ⓐ. For approx. 0.07 second, this monostable multivibrator is unstable and stops the IC1203 operation.



3) IC1203

This is a Johnson counter with five-stages which divides the 125 kHz clock pulse to 1/10 to make three pulses, such as gate, latch and reset.

The output of the monostable multivibrator is connected with the ENABLE terminal to control the 125 kHz clock-pulse. Again, the output of the monostable multivibrator is connected with the RESET terminal to keep each timing pulse in order. The output at terminal 11 is a trigger to make the monostable multivibrator of IC1202 unstable and stop the IC1203 operation as described in 2) IC1202.



4) IC1204

a) 1/2 IC1204

When the VFO output frequency becomes less than 2.456 MHz or more than 3.455 MHz, the MHz digits of the received signal frequency change, and the output of IC1207 activates IC1204 to send a blanking signal to the decoder drivers (IC1208 to IC1210). When the blanking signal is 1, only three dots appear on the kHz digits of the SW frequency counter.

b) 2/2 IC1204

A latch for storing the output of ½ IC1204. The latch is constituted by a D flip-flop. The latch pulse is applied to the CLOCK terminal. The R and S terminals are at 0 level.

5) IC1205 to IC1207

These constitute the ripple down-counter which can be preset. 455 is a preset value in DSB mode, 454 in USB mode, and 456 in LSB or CW mode. The 3.455 to 2.456 MHz of the VFO output is converted to the indication of 000 to 999 on the SW frequency counter.

6) IC1208 to IC1210

These constitute the latch, BCD-7 segments decoder and LED driver. These hold the output of the counter (IC1205, IC1206 or IC1207) every time a latch pulse arrives, and simultaneously convert BCD into the 7-segments indicated by the LED. The LED indication is eliminated by setting the B.1 input of the decoder to 0 level.

7) LED1201 to LED 1203

These are common cathode type LEDs. The LED lights when high-level voltage is applied to its anode. The segment showing a dot lights when a high voltage comes from the OR GATE composed of Q1208 and Q1209.

4. SW RF FILTER

1) Filter for External SW Antenna

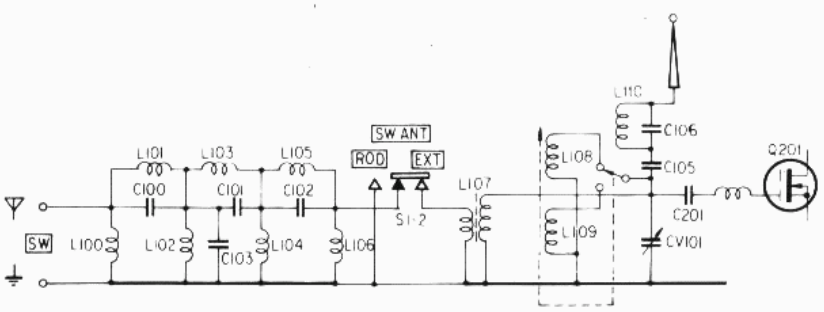
When an external antenna is used to boost the strength of a desired frequency range, the input of unwanted frequencies will also be increased. Many of the unwanted MW frequencies are especially strong, and if harmonics of MW frequencies are permitted to reach Q201 in the RF amplifier, they may interfere with SW reception. To prevent this, a sharp bandpass filter (low-cut filter) is included before the RF amplifier.

2) Antenna Tuning

The ANTENNA TUNING knob for adjusting the SW antenna circuit is a relatively new feature in radio equipment. This system is provided since it is difficult to obtain correct tracking between the antenna tank circuit and the local oscillator, and since in the usual wide-range bandpass type radio, optimum selectivity can not be obtained.

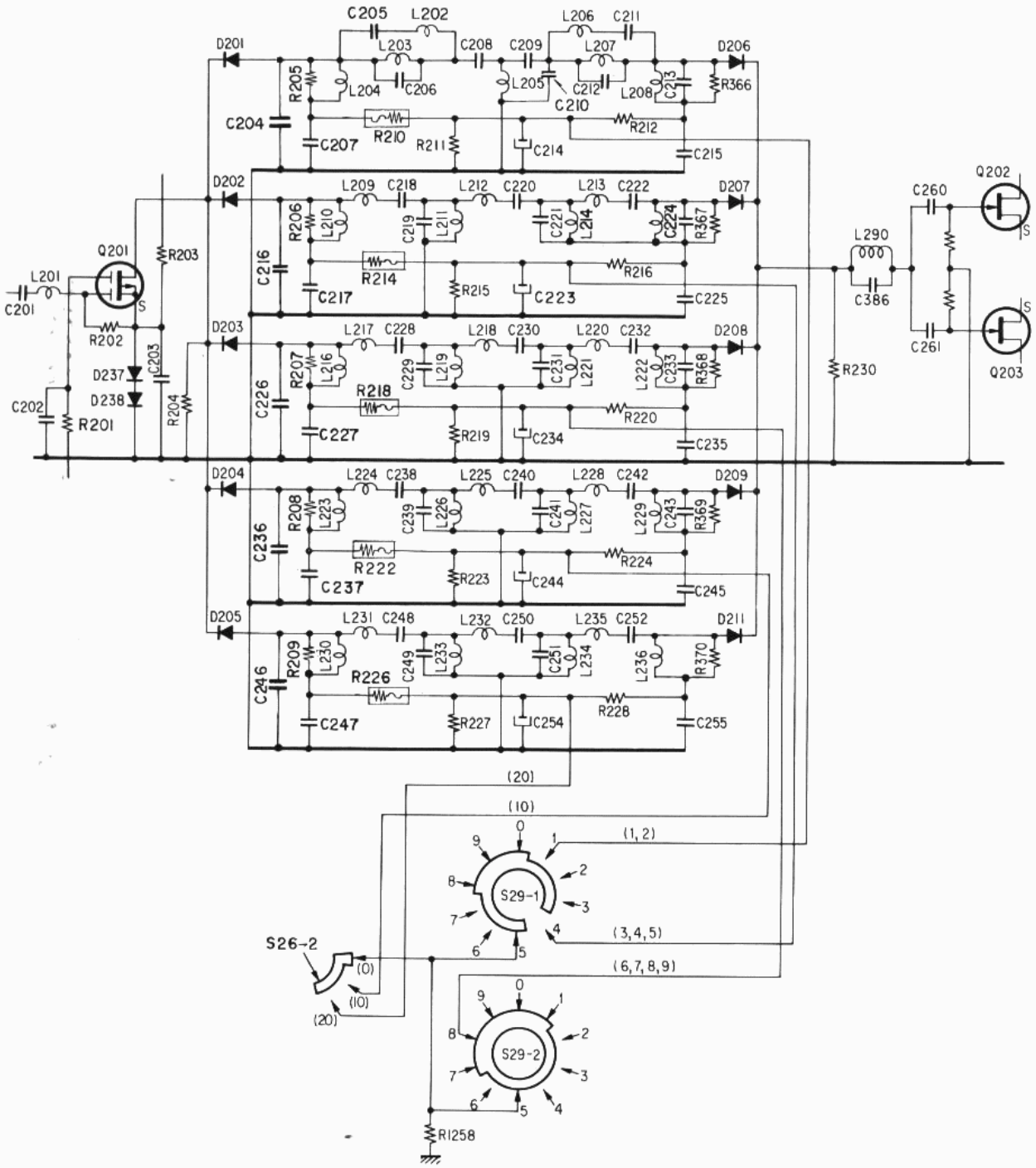
Also, since one coil can not cover the whole 1.6 to 30 MHz range, a coil switching at the 7 MHz position has been provided.

L110 and C106 in the telescopic antenna circuit constitute a trap for TV signals.



3) RF Filter Switching

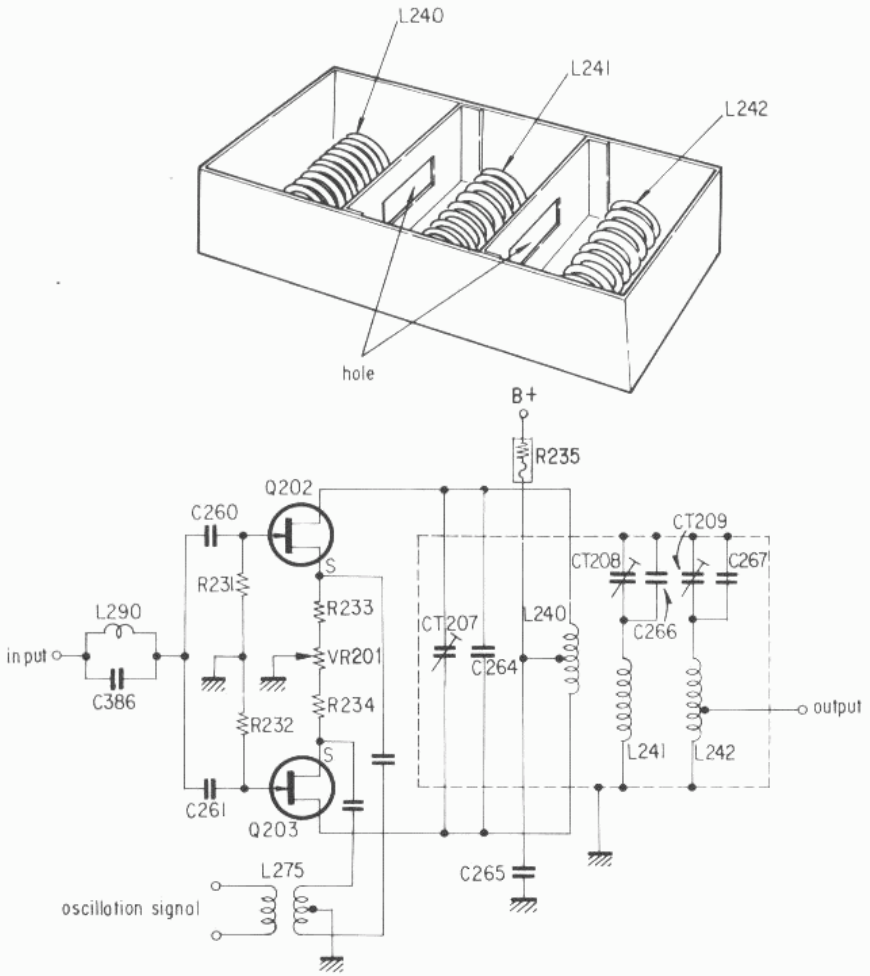
The SW RF filter in this set is of the bandpass type. However, the reception range is wide, extending from 1.6 to 30 MHz, so five sets of bandpass filters are selected for the appropriate reception bands. Switching is effected by the SW BAND SELECTOR switch, with a 12 V supply turning D201 to D211 on and off. S29-1 and S29-2 in the diagram is in the 9 MHz position, so it would be turned to the right (clockwise) successively to positions 0, 1, 2, etc. Again, S26-2 is in the 0 position, and would be turned similarly to positions 1, 2. It follows that D201 and D206 are on for 1 to 3 MHz, D202 and D207 are on for 3 to 6 MHz, D203 and D208 are on for 6 to 10 MHz, D204 and D209 are on for 10 to 20 MHz, and D205 and D211 are similarly on for 20 to 30 MHz, effecting the bandpass filter switching.



5. BALANCED TYPE SW FIRST MIXER

The input signal from the antenna is initially filtered by the antenna-tuning circuit, and then passes through the RF amplifier and a subsequent bandpass filter to remove unwanted frequency components of the input, the is fed to the first mixer. However, if any unwanted frequency component which is to be removed by the RF filter is present at high signal strength, it may be impossible for the RF filter alone to eliminate it, and it may be passed on to the input signal. If they do not match, the phase coincides with the frequency of the first i-f signal, the conventional single type mixer would pass on the unwanted frequency component and it would enter the first i-f circuit. In such a case, no subsequent circuit would be able to eliminate it, and it would persist as interference. In the balanced type mixer, however, the input signal does not appear in the same form at the output (it undergoes frequency conversion, and appears in the converted form).

Let us assume that the first i-f signal of 45.145MHz enters the input of the mixer shown in the diagram. This signal is in the same phase at both Q202 and Q203 gates, and also appears in the same phase at their drains. But it appears in the opposite phase at L240, so that it is cancelled out, and does not appear at the output. The VR201 between the sources of Q202 and Q203 is for adjustment to ensure that the two FETs operate with the same gain and cancel the signal out completely. However, the local oscillator signal is applied in the opposite phase to Q202 and Q203, so that the frequency-converted signal appears at the drains in the opposite phase. The signal level is doubled at L240, so that a higher-level i-f output signal appears at the output. Further, L240 to L242 are arranged as shown in the diagram, forming a triple-chain M-coupled filter, coupled through the holes in the shield case.



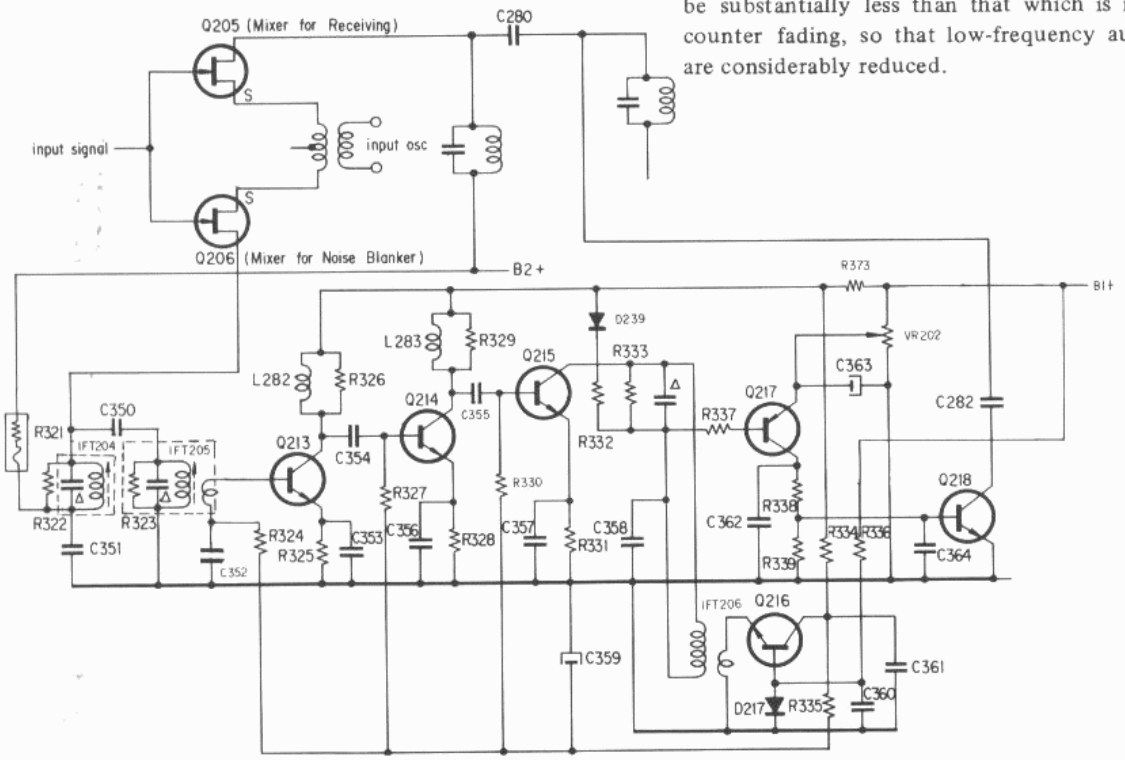
6. NOISE BLANKER

High-level pulse noise such as automobile ignition noise is both highly audible and extremely irritating. In order to remove this, a noise limiter is often used. To secure an even more effective removal of pulse noise, a noise blanker is used.

The diagram shows the noise blanker circuit. The i-f signal derived from the noise blanker mixer is adequately amplified by Q213, Q214 and Q215, and at the same time a powerful AGC is applied to level out the signal amplitudes. When no high-amplitude signal appears, Q217 is in the cut-off state, and no base current flows through Q218, so that the impedance of Q218 is high. When a pulsative (noise) signal appears, operation is as follows.

The AGC does not respond to the pulse signal. Therefore, the pulse is applied at a sufficiently high level to Q217, so that Q217 goes on. With Q217 on the pulse current also flows in the base of Q218, and Q218 goes on, and the i-f signal is passed to ground via C282 and Q218, so that the pulse noise portion is eliminated. The deleted section of the i-f signal is largely compensated for in the following tank circuit, detector, and the integrating circuit of the AF section, so that the effect is not obtrusive.

Q216 in the diagram is the AGC amplifier. Because of the common-base circuit, the base circuit has a constant voltage supply via D217. If a voltage higher than the base potential is applied to the emitter, Q216 rapidly cuts off, and powerful AGC is applied. Again, the AGC time constant is chosen to be substantially less than that which is required to counter fading, so that low-frequency audio signals are considerably reduced.



a) input signal

b) waveform after noise limiter

c) waveform after noise blanker

7. CIRCUITS FOR SSB AND CW RECEPTION

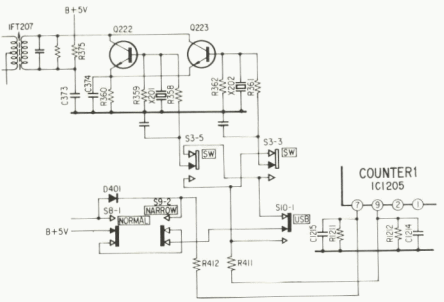
1) BFO

Two crystal oscillators, one for USB and the other for LSB, are used in the BFO of this set to ensure reception stability. These oscillators are switched by changing the biases of Q222 and Q223 with S10-1, S3-3 or S3-5 as required. In SW SSB reception, this set operates as a double superheterodyne receiver and in MW/LW SSB reception, as a single superheterodyne receiver. The SSB carrier waves are therefore reversed as necessary with S3-3 and S3-5. The oscillator frequency of Q222 is 453.5 kHz and that of Q223 is 456.5 kHz. The signal produced in this way is injected into the SSB detector as a carrier wave, but because this frequency is not 455 kHz, an accurate display of the frequency is not possible by VFO frequency counting as in AM mode. In order to obtain an accurate display of this frequency, 1.5 kHz must be added or substracted.

The counter of this set is the 455 kHz preset (programmable) down-counter. Here, for USB, this presetting must be made to 454 kHz, and for LSB, it must be preset to 456 kHz, in order to obtain accurate frequency readings. (The counter does not read 0.5 kHz intervals, so the preset need only be made to the nearest 1 kHz.)

The switching of the preset down-counter operates as follows. During A3 reception, either S8 or S9 is depressed and S10 to S12 are not depressed, so that the current flows from the 5 V power supply to terminal 7 of IC1205 via S8-1 and then to either D401 or S9-2. This current gives the counter instruction, and the preset goes to 455 kHz.. In LSB mode, the current goes to terminal 9 of IC1205 via S8-1, S10-1 and R411, and gives the counter instruction for the 456 kHz preset. In USB mode, there is no instruction for the counter from this circuit, and the counter is preset to 454 kHz.

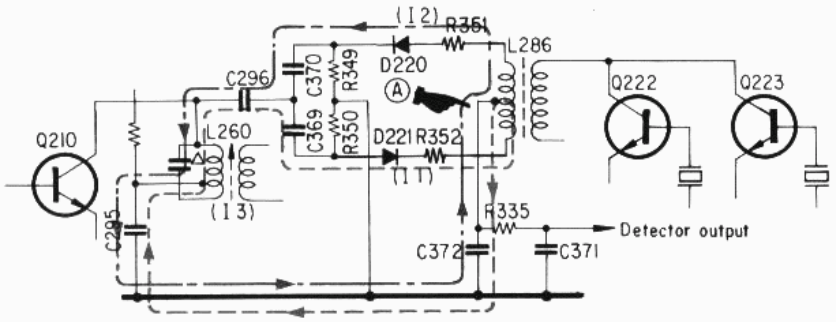
In CW mode, the BFO utilizes the LSB oscillator. The preset frequency is 456 kHz. Therefore, when the beat frequency is 1 kHz, accurate tuning is obtained. If the beat frequency is a little less than 1 kHz, the frequency indication will be more accurate. The beat frequency is usually 800 kHz. Under these conditions the set is not accurately tuned, but the frequency difference is allowable considering the i-f bandwidth.

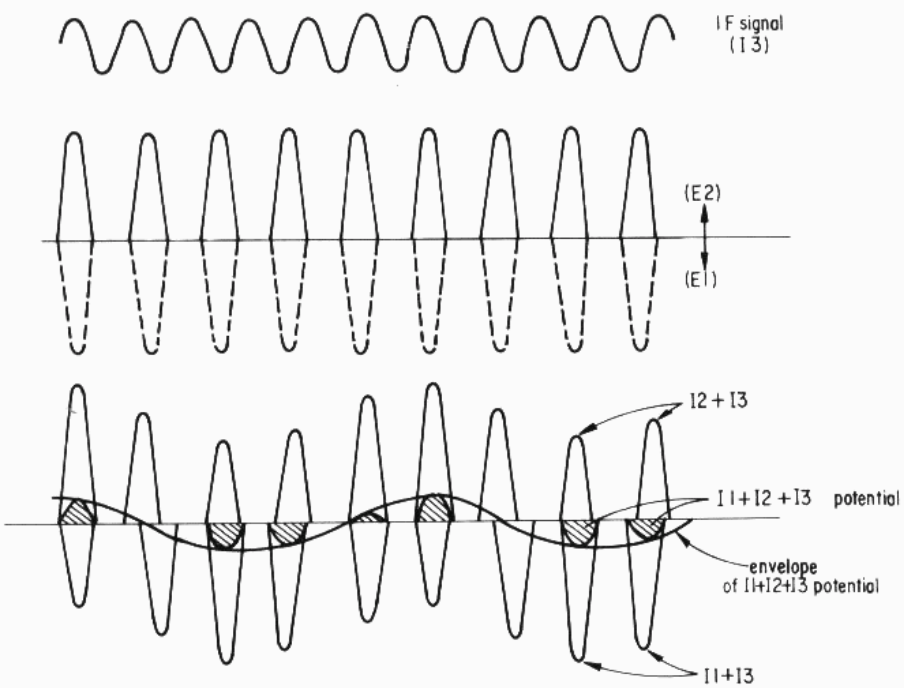


2) Product Detector

The oscillator output generated by Q222 or Q223 is applied to the secondary winding of L286, and induced currents I1 and I2 flow in the detector-side winding of L286. I1 and I2, under the action of D220 and D221, only flow for one half cycle of the sine wave. At this time the current develops a potential between the center tap Ⓐ of the primary winding of L286 (for deriving the detector output) and ground: I1 generates E1, and I2 generates E2. However, these potentials are of the same level but opposite polarity, so that when there is no i-f signal they cancel out and no potential is produced. When an i-f signal I3 (*Note) comes in, the beating between I1 and I3, and between I2 and I3, appears as a beat difference potential at tap Ⓐ. This potential is integrated via R335, C372 and C371 to result in an audio signal. This method of detection uses what is known as a balanced detector, where the currents I1 and I2 which flow through L260 cancel out, so that interference does not occur in i-f circuit.

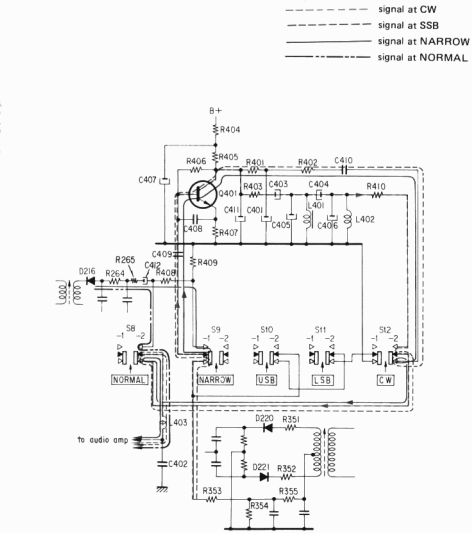
*Note: The I3 in the diagram is a part of the i-f signal when an SSB wave is being received, with continuous modulation by a signal frequency at the same level. In other words, this signal may be thought of as the same as the i-f signal when a CW signal is being received.





3) AF Amplifier Q401

Generally, the audio frequency range of a SSB transmission is not as wide as that of a DSB. After demodulation, the intelligibility of the sound is more important than its HiFi features. So during SSB reception, the detected output is amplified by the AF amplifier, and then cut on the low and high sides by a filter. Even in the NARROW position there are no real problems with the tonal quality. The demodulated frequency in the CW is normally constant. The width of the band produced is very narrow, a sharp filter with a peak around 800 kHz being used.

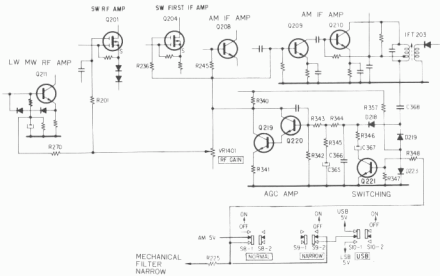


8. AGC CIRCUIT

In this set, the AGC time constant increases in the CW, LSB, USB and NARROW positions, but decreases in the NORMAL position. During reception of A3 with relatively high input levels in the NORMAL position, the faster AGC response time produces more stable and better sound output. In the SSB and CW modes, if the AGC time constant is low in the no-carrier portions the gain increases and a considerable amount of noise is heard from the speaker. Even during A3 reception, if the signal is weak, fading etc. produce sudden drops in level accompanied by considerable noise. And since the noise in weak signals is also a function of bandwidth, the NARROW position is most commonly used. Because of the reasons described above, the AGC time constant increases in the CW, LSB, USB and NARROW positions.

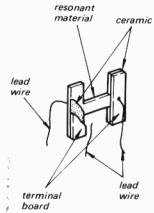
When the S8-1 (NORMAL) is switched off, Q221 is switched on as result of the bias signal sent to it from the 5 V power supply. Consequently, R346 and C367 inserted between the cathode of D218 and ground will increase the time constant.

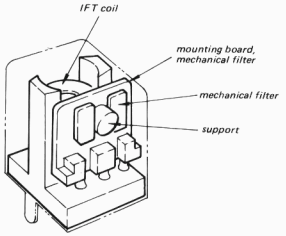
The RF GAIN control differs from the conventional manual gain control. The AGC circuit in the i-f stage is alone responsible for changing the gain in the RF amplifier. The reason for this is that if the gain is decreased in the first input circuit, the later stages will operate in the same way as during normal reception. So even if the gain is lowered during reception of strong signals, the output level of the speaker will remain fairly constant, and intermodulation can be minimized. The AGC circuit is also effective in reducing fading, which the conventional manual gain control is not able to do. The adjustable range of the RF GAIN is 40 dB.



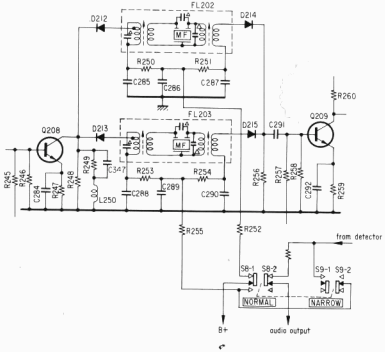
9. MECHANICAL FILTERS FL202 AND FL203

Mechanical filters have performance characteristics that make them useful as i-f filters, and for this reason they are widely used in communication equipment. In this set, mechanical filters of the type shown in the diagram (a) are used, with ceramic used to drive the resonant material. One of the mechanical filters consists of one element built into a drive-type IFT and the other consists of one element built into an output-type IFT. As shown in the diagram (b), two IFTs have been provided to enable switching between NARROW and NORMAL operation. This gives the receiver different bandwidths by switching the two mechanical filters. The bandwidths for 6 dB are 7 kHz for FL202 and 4 kHz for FL203 as shown in the diagram (c).

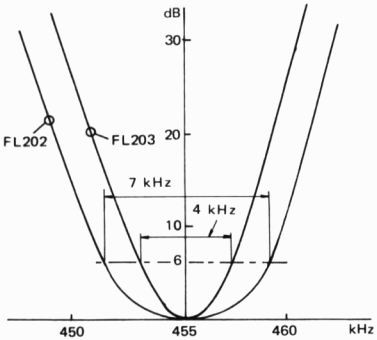




(a) Mechanical filter structure



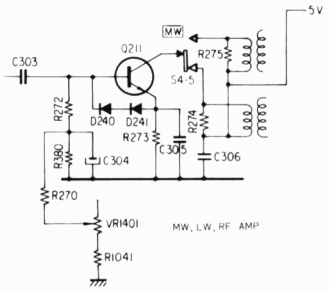
(b)



(c) Typical characteristic curve

10. Q211 IN MW AND LW RF AMPLIFIER

When an external antenna is connected, very strong signals are often passed into the RF amplifier stage. As a result, reverse currents may flow back from the base to the emitter in Q211, and break down the transistor. This is avoided by inserting diodes D240 and D241 between the base and emitter. Any reverse currents will then be by-passed by the diodes. These diodes also serve to prevent distortion due to amplitude limiting during the reception of strong signals.



11. POWER SUPPLY CIRCUIT

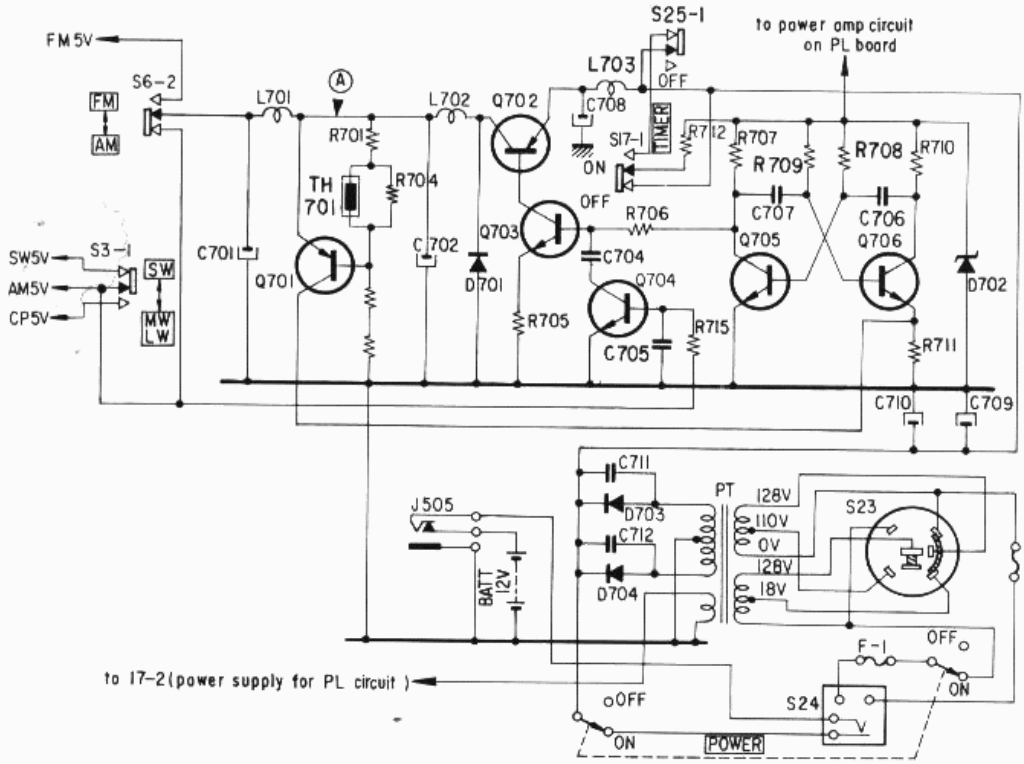
The regulator circuit in this set controls the output side voltage by changing the switching time of Q701. This is to reduce the power loss due to Q702.

Impedance control is used for the voltage regulation, and a 100 mA current is delivered. The primary voltage for this circuit is 12 V, and the secondary voltage is 5 V, so that the power consumed is (12−5) (V) x 100 (mA)=700 (mW), which is far from negligible.

Therefore, a switching control is provided for the regulator of this set. No current flows when Q702 is off, and when it is on, the impedance is extremely low, so that losses can be very significantly reduced. The conversion efficiency is 80%.

When the voltage at point Ⓐ slightly increases under the influence of load changes, the potential between the base and emitter of Q701 becomes large. This causes the collector current of Q701 to increase, with a corresponding increase in the emitter potential of Q706. Q705 and Q706 form a flip-flop, and generate square waves (approx. 2 kHz). Here, if the emitter potential of Q706 increases, the base potential also increases, decreasing the amount of discharge through C707. Therefore, the time for which Q706 is on is shortened. When Q706 is on, Q705 is off, causing Q703 and Q702 to be on. It follows that if the time that Q706 is on is reduced, the time that Q702 is on is also reduced, maintaining the secondary voltage at a constant level. On the other hand, when the secondary voltage drops, the emitter current of Q706 also drops, and the time for which Q706 is on becomes longer, so that Q702 is also on for a longer, time and the secondary voltage is maintained at the specified level. L702 is a smoothing choke coil. D701 is known as a catching diode, and it uses the starting current of L702 so that when Q702 is off, this diode passes a current through L702 which increases the efficiency of electrical supply utilization. The switching of Q702 acts with L701 and L705 to ensure that leakage of harmonics is prevented.

The waveform generated by the flip-flop oscillator is a high quality square wave. Square waves have inherently high levels of harmonics. It follows that if Q702 is driven in exactly the same way for LW and MW reception, the rod antenna will pick up the harmonic waves, resulting in interference. In order to prevent this, Q704 is put on during AM reception, a capacitor is inserted between the base of Q703 and ground, and the square waves are smoothed to prevent the generation of harmonics. However, for FM reception, the frequencies of reception are high, and the presence of such harmonics presents no problems. Under that condition, Q704 is set to off to increase the efficiency of the regulator.



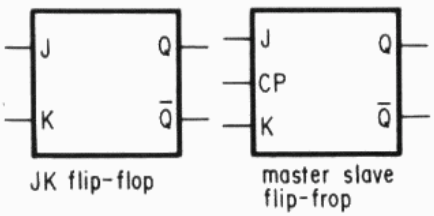
12. DIGITAL IC SYMBOLS AND OPERATIONS

1) Flip-Flop

The flip-flop circuits in this set have two logical conditions which are determined according to external instruction signals. They form a kind of memory circuit.

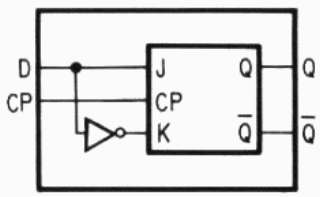
a) JK Flip-Flop

When the J input of the JK flip-flop is 1, the Q output is also 1, but when the K input is 1, Q becomes 0. And when the J and K inputs are of different polarities, the original status is reversed. The JK flip-flops shown below are called clocked JK flip-flop circuits because of the additional clock (CP) input terminal. With J and K inputs, the clocked JK flip-flop status does not change, but when clock inputs are received, the type of J and K inputs will determine the output. This principle is adopted in IC1002 where the CP signal is divided to 1/2 when the J and K inputs of the clocked JK (master-slave) flip-flop are both 1.



b) D Flip-Flop

In this kind of flip-flop, the J and K inputs are connected to each other via an inverter. The combined input terminal for J and K inputs is called the D input, and is capable of determining the status of outputs Q and $\bar{Q}$ during the input of CP signals.



This principle is employed when using CP inputs as strobes. When the CP input is 1, the D input appears at the output unchanged until the next CP (strobe) signal arrives. This kind of action is called "latch", and is used in IC1201 to IC1208. IC1201 and IC1204 use two D flip-flop circuits, and have SR terminals. The SR terminal becomes 0 level for operating as a D flip-flop.

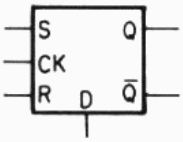
D	CP	t_{n-1} Q	t_n Q
1	⌐¯	0	1
1	⌐¯	1	1
0	⌐¯	0	0
0	⌐¯	1	0

The Q of the flip-flop output can be reversed every rise time of CP when grounding the $\bar{Q}$ and D terminals. This kind of flip-flop is called a T flip-flop.

c) RS Flip-Flop

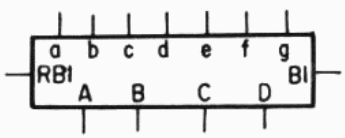
The RS flip-flop status is determined by the S (set) and R (reset) input signals. If either S or R input signal is 1, the status is maintained. But when the S input is 0, $\bar{Q}$ becomes 0, and Q becomes 1. The S input then reverts to 1, but the Q and $\bar{Q}$ states remain unchanged. On the other hand, when R input is 0, Q becomes 0, and $\bar{Q}$ becomes 1. When the R and S inputs are both 0 or 1, the output is not designated.

S	R	Q
1	0	1
0	1	0
0	0	NO CHANGE
1	1	NOT PERMISSIBLE



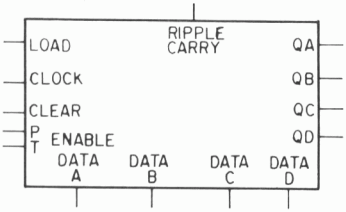
2) Decoder

The decoder converts the BCD code of the counter output into decimal notation for the LEDs. The terminals A to D shown below are for counter inputs, while a to g are the outputs for LED signals. BI is the blanking input for extinguishing the LEDs, while RBI is the ground connection for blanking when the counter is 0.



3) Programmable Counter

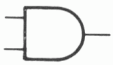
This counter can be preset via the inputs at the DATA A to DATA D. The counter is reset by inputting a pulse signal at the LOAD, but will not operate if there is no input at the ENABLE. The counter outputs appear at the QA to QD, with the output for digit increase at the RIPPLE CARRY.



4) AND Gate

An output of 1 only appears when both inputs are 1.

Note: 0 for L level and 1 for H level is referred to as positive logic, while 1 for L level and 0 for H level is called negative logic.



5) OR Gate

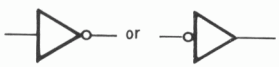
An output of 1 appears if either input is 1.

6) Buffer

Symbol for buffer amplifier.

7) Inverter

Symbol for phase inverter.



○ indicates phase inverting.

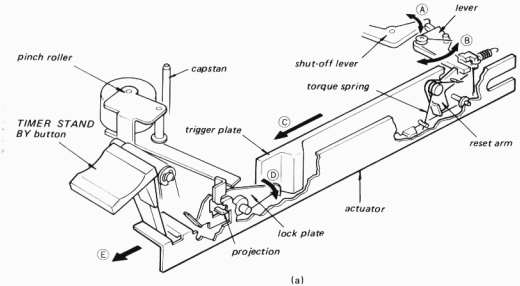
TAPE RECORDER SECTION

1. TIMER STAND-BY MECHANISM

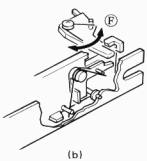
In this set, a TIMER STAND-BY mechanism is provided to operate the tape recorder automatically at the desired time. The mechanism also prevents the pinch roller and capstan from deforming from prolonged contact.

The diagram (a) shows the TIMER STAND-BY setting. At the desired time, the power supply works to rotate the motor, and then the shut-off lever moves to release the lock plate by the projection of the actuator assembly (Operation: Ⓐ to Ⓓ). At this time, the actuator assembly moves toward Ⓔ and sets the reset arm as shown in the diagram (c). After this, the lever continues to move as shown by Ⓖ, but has no influence on the actuator assembly.

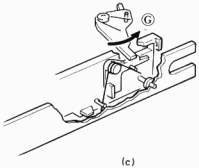
If the TIMER STAND-BY mechanism is set when the lever is as shown in the diagram (b), the lever moves toward Ⓕ at the desired time. But after this, the mechanism operates as described above.



(a)



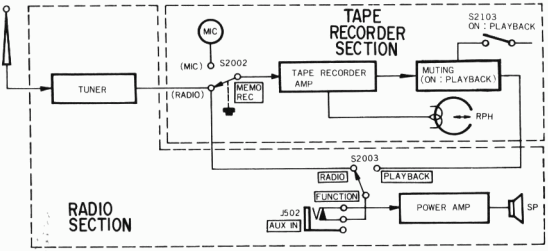
(b)



(c)

2. CONNECTION OF THE TAPE RECORDER AND RADIO

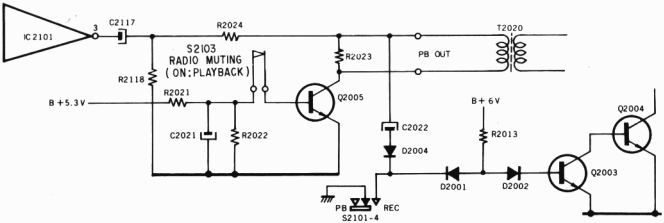
The block diagram is shown below. A signal from the microphone can be recorded only when S2002 is pressed. A signal from J502 can not be recorded.



3. RECORD MUTING

If a signal should appear at the speaker when recording through the microphone, howling would occur. To prevent this, the RECORD MUTING circuit is inserted in the output circuit.

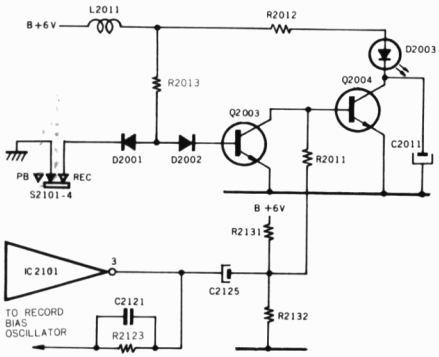
The diagram below shows the RECORD MUTING circuit. Except in playback mode, when S2103 becomes on, the output of IC2101 flows to the power amplifier through T2020. To complete the muting, the signal circuit is grounded via C2022, D2004 and S2101-4 in record mode.



4. LED AMPLIFIER

In record mode, a part of the IC2101 output goes to Q2004 via C2125 and R2011, and makes D2003 flicker to indicate recording. This is not necessary in playback mode, so the signal is muted as follows.

In playback mode, since the bias voltage is applied to Q2003 via R2103 and D2002, Q2003 is on. The base of Q2004 is grounded, so D2003 does not flicker. In record mode, since the bias circuit of Q2003 is grounded via D2001 and S2101-4, Q2003 is off. Therefore, Q2004 is biased for class B operation and flickers with the variations of the audio input signal.



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Printed in Japan

K4XL's  BAMA

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